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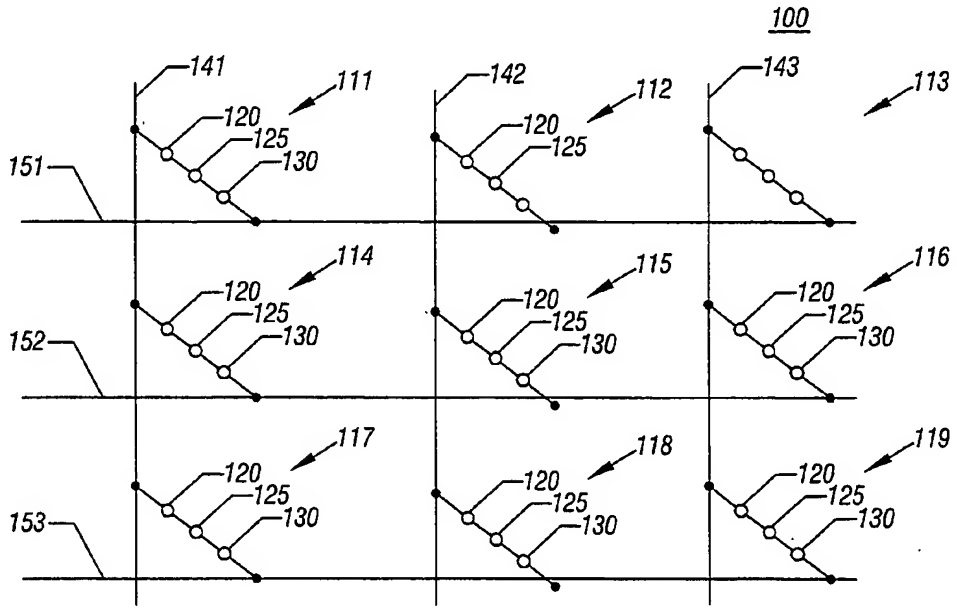
(54) Title: MEMORY AND ACCESS DEVICES



(57) Abstract: Briefly, in accordance with an embodiment of the invention, a memory (100) is provided. The memory (100) may include a memory element (130) and a first access device (120) coupled to the memory element (130), wherein the first access device (120) comprises a first chalcogenide material (940). The memory (100) may further include a second access device (125) coupled to the first access device(120), wherein the second access device (125) comprises a second chalcogenide material (920).

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Memory And Access Devices

Background

Phase change memory devices use phase change materials, i.e., materials that may be electrically switched between a generally amorphous and a generally crystalline state, for electronic memory application. One type of memory element utilizes a phase change material that may be, in one application, electrically switched between a structural state of generally amorphous and generally crystalline local order or between different detectable states of local order across the entire spectrum between completely amorphous and completely crystalline states. The state of the phase change materials are also non-volatile in that, when set in either a crystalline, semi-crystalline, amorphous, or semi-amorphous state representing a resistance value, that value is retained until changed by another programming event, as that value represents a phase or physical state of the material (e.g., crystalline or amorphous).

A transistor or a diode may be connected to the phase change material and may serve as a select device to access the phase change material during programming or read operations. The transistor or diode is typically formed in or on the top surface of a silicon single crystal substrate. Transistors may take up a relatively large portion of the memory chip, and therefore may increase the memory cell size, thereby adversely affecting the memory capacity and cost/bit of a memory chip.

Brief Description Of The Drawings

FIG. 1 is a schematic diagram illustrating a memory in accordance with another embodiment of the present invention; and

FIG. 2 is a cross-sectional view of a portion of the memory illustrated in FIG. 17 in accordance with an embodiment of the present invention;

FIG. 3 is a diagram illustrating a current-voltage characteristic of a memory cell; and

FIG. 4 is a diagram illustrating a current-voltage characteristic of a select device.

Detailed Description

Select device 120 may be used to access memory element 130 during programming or reading of memory element 130. Select device 120 may operate as a switch that is either "off" or "on" depending on the amount of voltage potential applied across the memory cell.

The off state may be a substantially electrically nonconductive state and the on state may be a substantially conductive state. For example, select device 120 may have a threshold voltage and if a voltage potential less than the threshold voltage of select device 120 is applied across select device 120, then select device 120 may remain "off "or in a relatively high resistive state so that little or no electrical current passes through the memory cell. Alternatively, if a voltage potential greater than the threshold voltage of select device 120 is applied across select device 120, then select device 120 may "turn on," i.e., operate in a relatively low resistive state so that electrical current passes through the memory cell. In other words, select device 120 may be in a substantially electrically nonconductive state if less than a predetermined voltage potential, e.g., the threshold voltage, is applied across select device 120. Select device 120 may be in a substantially conductive state if greater than the predetermined voltage potential is applied across select device 120. Select device 120 may also be referred to as an access device, an isolation device, or a switch.

In one embodiment, select device 120 may comprise a switching material such as, for example, a chalcogenide or an ovonic material, and may be referred to as an ovonic threshold switch, or simply an ovonic switch. The switching material of select device 120 may be a material in a substantially amorphous state positioned between two electrodes that may be repeatedly and reversibly switched between a higher resistance "off" state (e.g., greater than about ten mega-ohms) and a relatively lower resistance "on" state (e.g., about zero ohms) by application of a predetermined electrical current or voltage potential. In this embodiment, select device 120 may be a two terminal device that may have a current-voltage (I-V) characteristic similar to a phase change memory element that is in the amorphous state. However, unlike a phase change memory element, the switching material of select device 120 may not change phase. That is, the switching material of select device 120 may not be a programmable material, and as a result, select device 120 may not be a memory device capable of storing information. For example, the switching material of select device 120 may remain permanently amorphous and the I-V characteristic may remain the same throughout the operating life.

FIG. 1 is a schematic diagram illustrating an embodiment of memory 100. In this embodiment, memory cells 111-119 each include select device 120, a select device 125, and memory element 130. In this embodiment, the total snapback may be reduced to allow use of

a lower threshold memory element. For example, if the total V_{TH} for the pair of ovonic switches is about two volts, the individual V_{TH} of each switch may be about one volt by appropriate choice of the switching material thickness. If the V_H of each is, for example, 0.8 volts, the snapback may be reduced to about 0.4 volts total from about 1.2 volts if a single device is used. Such a stacked series set of switch devices may reduce the tendency to disturb a bit during read. Such a stack may be comprised of one switch, two switches, or more switches in series with the memory element, all placed between the row and column line assisting reliable memory selection and operation.

As is illustrated, memory element 130 and select devices 120 and 125 are connected in a serial arrangement. In one embodiment, select devices 120 and 125 may be ovonic switches and memory element 130 may be an ovonic memory.

Turning to FIG. 2, an embodiment of a memory cell (e.g., 115) of memory 100 is illustrated in accordance with another embodiment of the present invention. Memory cell 115 may comprise substrate 240, insulating material 260 overlying substrate 240, and conductive material 270 overlying insulating material 260. Conductive material 270 may be an address line (e.g., row line 152). Above conductive material 270, electrode 340 may be formed between portions of insulating material 280. Over electrode 340, sequential layers of a memory material 350, electrode material 360, a switching material 920, an electrode material 930, a switching material 940, an electrode material 950, and a conductive material 980 may be deposited to form a vertical memory cell structure. Conductive material 980 may be an address line (e.g., column line 142).

In the embodiment illustrated in FIG. 2, select devices 125 and 120 are formed over memory element 130 to form a serially coupled, thin film vertical structure or vertical stack. In alternate embodiments, memory element 130 may be formed above select devices 120 and 125 or memory element 130 may be formed between select devices 120 and 125 to form a serially coupled, thin film vertical structure. In the embodiment illustrated in FIG. 2, select devices 120 and 125 and memory element 130 may be formed using thin film materials, and the vertical stack may be referred to as a thin film vertical stack.

In the embodiment illustrated in FIG. 2, memory material 350 and electrodes 340 and 360 may form memory element 130. Memory material 350 may be an ovonic material or a chalcogenide material and may be referred to as an ovonic memory. Switching material 920

and electrodes 360 and 930 may form select device 125. Switching material 920 may be formed using similar materials and similar manufacturing techniques used to form switching material 220 described herein. Switching material 940 and electrodes 930 and 950 may form select device 120. Switching material 940 may be formed using similar materials and similar manufacturing techniques used to form switching material 220 described herein. In alternate embodiments, switching materials 920 and 940 may be composed of the same material or different materials. For example, in one embodiment, switching material 920 may be composed of a chalcogenide material and switching material 940 may be composed of another different chalcogenide material.

In one embodiment, select devices 120 and 125 may be ovonic switches and memory element 130 may be an ovonic memory and memory cell 115 may be referred to as an ovonic memory cell. As discussed above, an example of an I-V characteristic for select device 120 is shown in FIG. 4. Select device 125 may have an I-V characteristic similar to that illustrated in FIG. 4.

Turning to FIG. 3, an example of an I-V characteristic of memory cell 115, which may include memory element 130 and select devices 120 and 125 in this embodiment, is shown. The holding voltage of memory cell 115, labeled V_H, may result from the holding voltages of select devices 120 and 125 and memory element 130. The threshold voltage of memory cell 115 may be equal to the combined threshold voltages of memory element 130 and select devices 120 and 125.

As may be appreciated from the discussion herein, the threshold voltage of a select device or an ovonic switch may be determined by the thickness or alloy composition of the switching material of the ovonic switch and the holding voltage of an ovonic switch may be determined by the composition of the electrodes contacting the switching material of the ovonic switch. Accordingly, in one embodiment, the snapback voltage, i.e., the voltage difference between the threshold and holding voltages of an ovonic switch, may be reduced by reducing the thickness of the switching material and using a particular type of electrode.

For example, referring to select device 120 illustrated in FIG. 2, if electrodes 930 and 950 are carbon layers and if the thickness of switching material 940 is about 200 Å, then the holding voltage of select device 120 may be about one volt and the threshold voltage of select

device 120 may be about 1.2 volts. In this example, the snapback voltage may be about 0.2 volts, which is the difference between the holding and threshold voltages of select device 120.

In the embodiment illustrated in FIG. 2, memory cell 115 may include two ovonic switches serially coupled to an ovonic memory to decrease the voltage difference between the holding voltage and the threshold voltage of a memory cell when higher switching and holding voltages are desired. In other words, rather than using one ovonic switch, two ovonic switches may be serially coupled to an ovonic memory to decrease "snapback" of a memory cell, i.e., reduce the voltage difference between the threshold and holding voltages of an ovonic memory cell when higher switching and holding voltages are desired.

In one embodiment, electrodes 360, 930, and 950 may be carbon, the thickness of switching material 920 may be about 200 Å, and the thickness of switching material 940 may be about 200 Å. In this embodiment, the threshold voltage of select device 120 may be about 1.2 volts and the holding voltage of select device 120 may be about one volt. The threshold voltage of select device 125 may be about 1.2 volts and the holding voltage of select device 125 may be about one volt. If the threshold voltage of reset/set memory element 130 is about 0.8/0.0 volts, then the threshold voltage of memory cell 115 may be about 3.2/2.4 volts for memory cell 115 in a reset state and set state, respectively, which is the combined threshold voltages of memory element 130 and select devices 120 and 125. That is, a voltage potential of greater than about 3.2 volts may be applied across memory cell 115 to "turn on" select devices 120 and 125 and conduct current through memory cell 115. A voltage of greater than about 3.2 volts may be applied across memory cell 115 by applying a voltage potential of greater than about 3.2 volts to column line 142 and a voltage potential of about zero volts to row line 152.

In this example, to program a selected memory cell, e.g., memory cell 115, a voltage of about 1.8 volts may be applied to unselected column and unselected row lines, e.g., lines 141, 143, 151, and 153. A voltage of greater than about 3.2 volts may be applied to a selected column line, e.g., 142, and zero volts may be applied to a selected row line, e.g., row line 152. In this example, after select devices 120 and 125 "turn on," then due to snapback, the voltage drop across memory cell 115 may be reduced from about 3.2 volts to about 2.0-2.8 volts depending on the cell's memory state and current provided by the column. Then, information may be stored in memory element 130 by forcing current through memory cell

115 while assuring that the selected column line remains within about 2.4 volts of the unselected row lines biased at about 1.8 volts so that unselected memory cells are not disturbed. That is, the column may not be allowed to be higher than about 4.2 volts during programming.

FIG. 3 may be used to graphically illustrate this example, wherein for the full memory cell (all 3 components taken together), V_{TH} is 3.2/2.4 volts for a reset state and set state, respectively, and V_H is 2.8 volts. The current through memory cell 115 is near zero amperes until the threshold voltage, V_{TH}, of, for example, about 3.2 or 2.4 volts is exceeded, depending on whether the memory cell is in a reset or set state respectively. Then the voltage across memory cell 115 drops to (for a reset bit) or climbs to (for a set bit) the holding voltage, V_H, of, for example, about 2.8 volts, as the current is increased.

To read the value of the information stored in the selected memory cell, in this example, a voltage of about 2.8 volts may be applied across memory cell 115. The resistance of memory element 130 may be sensed to determine if memory element 130 is in a low resistance crystalline, "set" state (e.g., less than about 10,000 ohms) or if memory element 130 is in a high resistance amorphous, "reset" state (e.g., greater than about 10,000 ohms).

In another embodiment, to read the value of the information stored in the selected memory cell, a voltage of about 2.8 volts may be applied across memory cell 115 by applying 2.8 volts to the selected column and zero volts to the selected row and 1.4 volts to all other unselected rows and columns. The resistance from the selected column to the selected row may be sensed to determine if memory element 130 is in a low resistance crystalline, "set" state or if memory element 130 is in a high resistance amorphous, "reset" state. In this embodiment, the series select devices may not "turn on" for the case of a reset state, thus also providing a high resistance between the selected column and selected row.

It should be understood that the above examples are not a limitation of the present invention. Other holding voltages and threshold voltages may be achieved to alter the snapback of memory cells by altering the thickness of switching materials 920 and 940 and the compositions of electrodes 360, 930, and 950. One advantage of reducing the snapback of a memory cell is that capacitive displacement current through-the memory cell may be reduced, thus reducing the tendency to disturb a bit into a different state while reading.

In other embodiments, memory cell 115 illustrated in FIG. 2 may be arranged

differently and include additional layers and structures. For example, it may be desirable to form isolation structures, barrier layers, peripheral circuitry (e.g., addressing circuitry), etc. The memory cell may instead be a ferro-electric or ferro-magnetic material with different phases programmed by different currents or polarity, and that result in different impedances when programmed to the different states. Alternately, the memory cell may be any other material or device benefiting from a small access device. It should be understood that the absence of these elements is not a limitation of the scope of the present invention.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

What is claimed:

1. An apparatus, comprising:

a memory element;

a first access device coupled to the memory element, wherein the first access device comprises a first chalcogenide material; and

a second access device coupled to the first access device, wherein the second access device comprises a second chalcogenide material.

2. The apparatus of claim 1, further comprising a vertical structure over a substrate, wherein the vertical structure comprises the first access device, the second access device, and the memory element serially coupled to each other.

3. The apparatus of claim 1, wherein the first access device, the second access device, and the memory element are formed using thin film materials.

4. The apparatus of claim 1, wherein the second access device is over the first access device, and the first access device is over the memory element.

5. The apparatus of claim 1, wherein the first select device includes a switching material that is in a substantially amorphous state and is adapted to be repeatedly and reversibly switched between a higher resistance state and a relatively lower resistance state by application of a predetermined voltage or current.

6. The apparatus of claim 1, wherein the memory element comprises a phase change material that is capable of being programmed into one of at least two memory states by applying a current to the phase change material to alter the phase of the phase change material between a substantially crystalline state and a substantially amorphous state, wherein a resistance of the phase change material in the substantially amorphous state is greater than the resistance of the phase change material in the substantially crystalline state.

7. The apparatus of claim 1, wherein the memory element comprises a memory material over a substrate and wherein the first chalcogenide material is over the memory material and the second chalcogenide material is over the first chalcogenide material.

8. The apparatus of claim 7, further comprising:

a first electrode between the memory material and the first chalcogenide material; and

a second electrode between the first chalcogenide material and the second chalcogenide material.

9. The apparatus of claim 8, wherein the first electrode and the second electrode are thin films of carbon.

10. The apparatus of claim 7, wherein the first chalcogenide material, the second chalcogenide material, and the memory material each comprise tellurium.

11. The apparatus of claim 7, wherein the first chalcogenide material is a material selected from the group consisting of silicon, tellurium, arsenic, germanium, and combinations thereof.

12. The apparatus of claim 7, wherein the memory material is a tellurium, antimony, germanium alloy.

13. An apparatus, comprising:

a first ovonic switch;

a second ovonic switch coupled to the first ovonic switch; and

a memory element coupled to the second ovonic switch.

14. The apparatus of claim 13, wherein the memory element, the first ovonic switch, and the second ovonic switch are formed using thin film materials.

15. The apparatus of claim 13, further comprising a vertical structure over a substrate, wherein the vertical structure comprises the first ovonic switch, the second ovonic switch, and the memory element serially coupled to each other.

16. An apparatus, comprising:
a memory material over a substrate;
a first electrode over the memory material;
a first chalcogenide material over the first electrode;
a second electrode over the first chalcogenide material; and
a second chalcogenide material over the second electrode.

17. The apparatus of claim 16, wherein the memory material, the first electrode, the first chalcogenide material, the second electrode, and the second chalcogenide material form portions of a vertical stack over the substrate.

18. The apparatus of claim 16, wherein the memory material, the first electrode, the first chalcogenide material, the second electrode, and the second chalcogenide material are each thin film materials.

19. An apparatus, comprising:
a memory cell having a holding voltage, wherein the memory cell comprises:
a memory element; and
at least two serially coupled access devices coupled to the memory element to increase the holding voltage of the memory cell.

20. The apparatus of claim 19,
wherein the memory element includes a phase change material; and
wherein a first access device of the two serially coupled access devices includes a first chalcogenide material and wherein the second access device of the two serially coupled access devices includes a second chalcogenide material.

21. The apparatus of claim 20, wherein the first chalcogenide material is different than the second chalcogenide material.

22. The apparatus of claim 19, wherein a first access device of the at least two serially coupled access devices, a second access device of the at least two serially coupled access devices, and the memory element are formed using thin film materials.

23. A system, comprising:

a processor;

a wireless interface coupled to the processor; and

a memory coupled to the processor, the memory including:

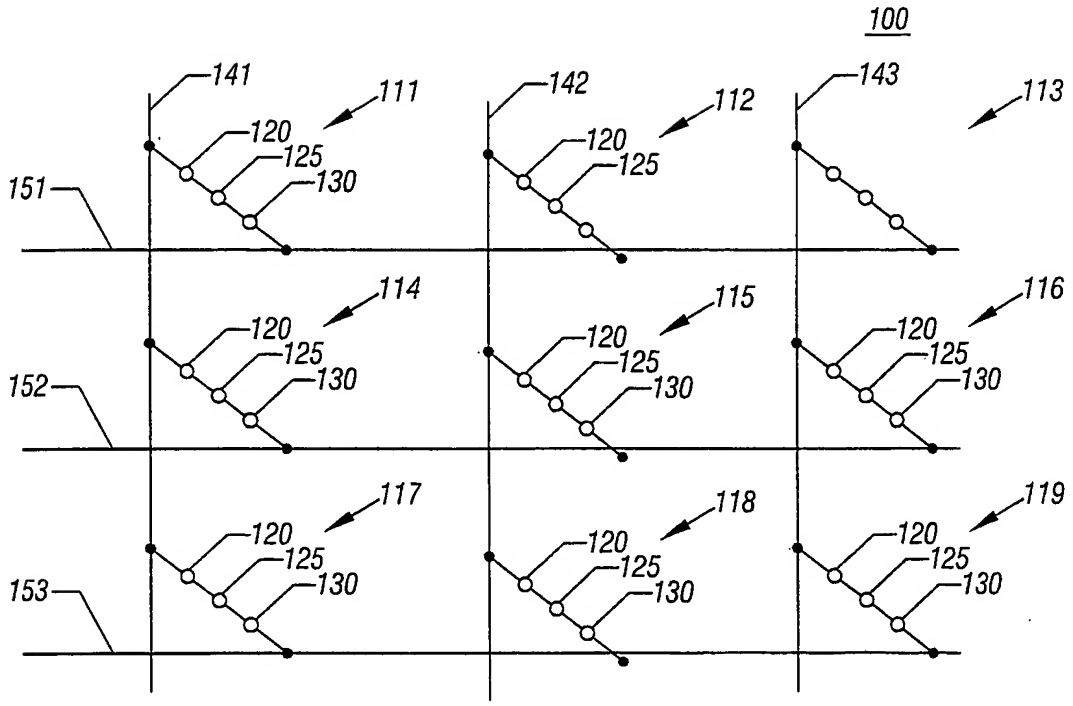
a memory element;

a first access device coupled to the memory element, wherein the first access device comprises a first chalcogenide material; and

a second access device coupled to the first access device, wherein the second access device comprises a second chalcogenide material.

24. The system of claim 23, wherein the memory element comprises a memory material over a substrate and wherein the first chalcogenide material is over the memory material and the second chalcogenide material is over the first chalcogenide material.

25. The system of claim 23, wherein the memory further comprises a vertical structure over a substrate, wherein the vertical structure comprises the first access device, the second access device, and the memory element serially coupled to each other.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125
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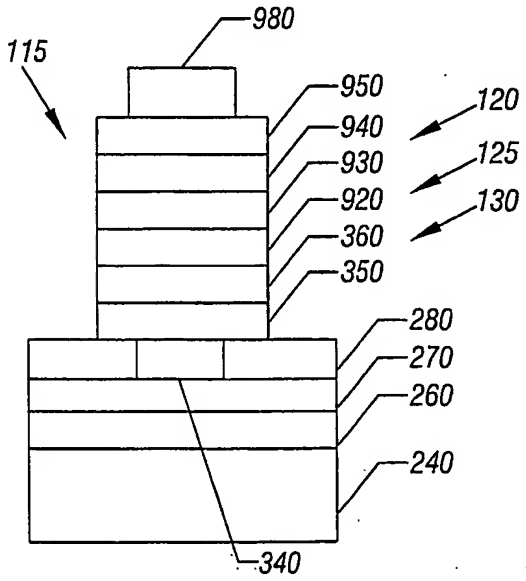
FIG. 1


980
115
950
940
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920
360
350
120
125
130
280
270
260
240
340

FIG. 2

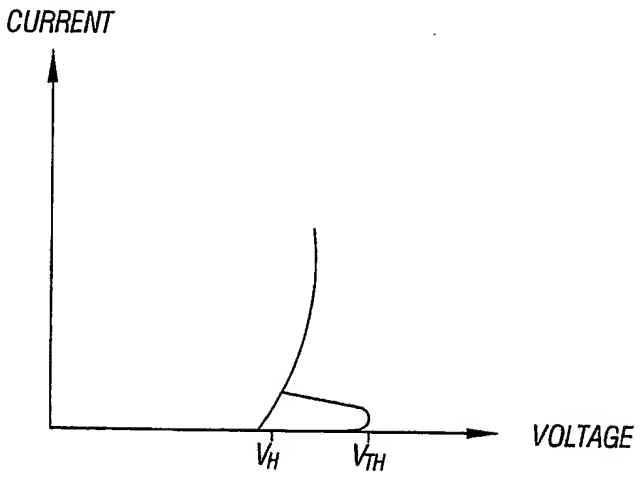

FIG. 3

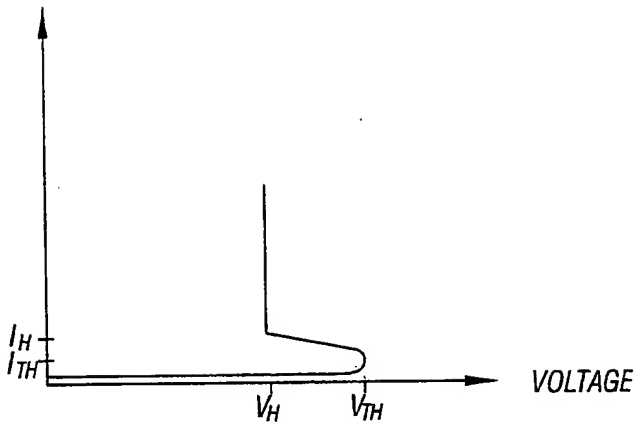

FIG. 4